ELIZADE UNIVERSITY, ILARA-MOKIN, ONDO STATE

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

FIRST SEMESTER EXAMINATION, 2020/2021 ACADEMIC SESSION

COURSE TITLE: ADVANCED CIRCUIT TECHNIQUES

COURSE CODE: EEE 517

EXAMINATION DATE: --TH MARCH, 2021

COURSE LECTURER: DR R. O. Alli-Oke

HOD's SIGNATURE

TIME ALLOWED: 2 HRS

INSTRUCTIONS:

1. ANSWER **QUESTION 1** AND ANY OTHER THREE QUESTIONS **(TOTAL OF 4 QUESTIONS)**
2. SEVERE PENALTIES APPLY FOR MISCONDUCT, CHEATING, POSSESSION OF UNAUTHORIZED MATERIALS DURING EXAM.
3. YOU ARE **NOT** ALLOWED TO BORROW CALCULATORS AND ANY OTHER WRITING MATERIALS DURING THE EXAMINATION.

## QUESTION #1 [21 marks]

a) Consider the Sample and Hold (S & H) circuit shown in the Figure 1. [10 marks]

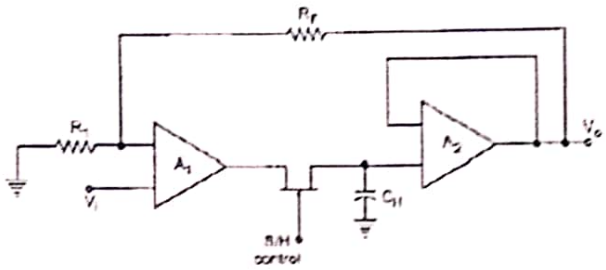


Figure 1: Sample and Hold (S & H) Feedback Circuit

i.) Briefly explain the operation of the S & H circuit shown in Figure 1.

ii.) Discuss 4 key characteristics or parameters that can be used in analysing its performance of S & H circuits.

iii.) Briefly explain why changing the position of the holding capacitor ($C_H$) in Figure 1 to a feedback position around op-amp A2 would provide shorter acquisition times ($t_{ac}$). Your answer should include the new S & H circuit.

b) Using a typical application, discuss the Analog to Digital Conversion Process. [11 marks]

## QUESTION #2 [13 marks]

a) Briefly explain the three common architectures for digital to analog (D/A) conversion [5 marks]

b) The current output of the 741 operational amplifier can be increased by cascading with a unity-gain op-amp. However, in order to meet power requirements, it is sometimes desirable to use discrete transistors to implement the unity gain stage. A 50mV RMS audio signal is to be amplified to drive an 8Ω-20W speaker. With the aid of a well-labelled schematic, describe an op-amp based power amplifier for this audio application that can handle negative load voltages, minimize cross-over distortion, and prevent break-out of oscillations. [8 marks]

## QUESTION #3 [13 marks]

a) Briefly discuss the operation of the phase-locked loop (PLL) shown in Figure 2. [7 marks]

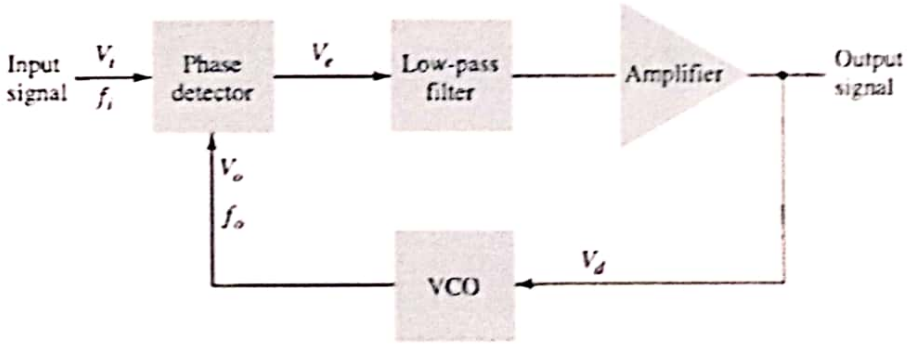


Figure 2: Phase-Locked Loop (PLL)

b) Consider an op-amp based 2-bit R-2R ladder D/A converter, where $V_1$ and $V_2$ correspond to the least significant bit (LSB) and most significant bit (MSB) respectively. The op-amp output is given by,

$$V_o = -\frac{V_1}{2} - \frac{V_2}{1}$$

Let the reference voltage $V_{ref}$ be 10 V. Determine the resolution and analog span/range of the D/A converter. [6 marks]

## QUESTION #4 [13 marks]

a) Write briefly on performance limitations related to PWM digital-to-analog conversion vis-à-vis DAC bandwidth, DAC speed, and effective DAC resolution. [5 marks]

b) Consider the op-amp circuit shown in Figure 3. [8 marks]

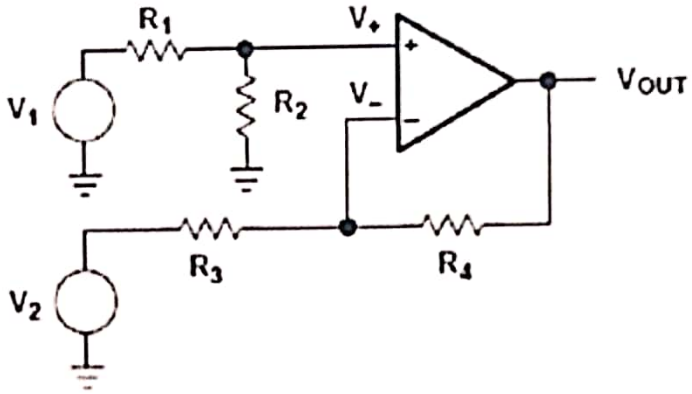


Figure 3: Operational Amplifier (Op-Amp) Circuit

i.) Show that the voltage gain of this op-amp circuit is given by $R_3/R_4$.

ii.) Identify and explain the purpose of this circuit. How does this circuit differ from instrumentation amplifiers?

## QUESTION #5 [13 marks]

a) Discuss the differences between impedance matching and impedance bridging. [5 marks]

b) Consider that the PIC17C42 microcontroller chip in Figure 4 can generate PWM frequencies of up to 62.5 $k$Hz. [8 marks]

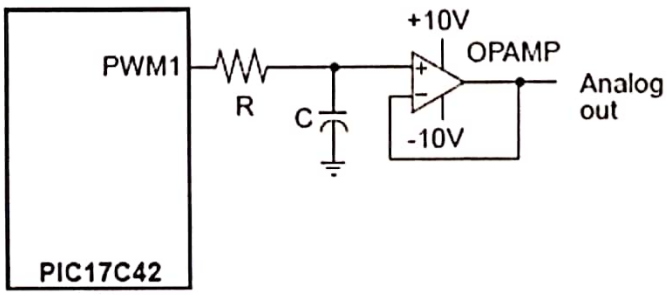


Figure 4: PWM Digital-to-Analog Conversion

i.) Design a simple RC low-pass filter to obtain an analog output from a pulse width modulated (PWM) speech signal of bandwidth 4 $k$Hz. Also, determine a suitable slew-rate spec of the op-amp. Make necessary assumptions.

ii.) With respect to your design in (i), briefly discuss with the aid of diagrams on how to improve the noise-rejection.

## QUESTION #6 [13 marks]

a) Explain the Nyquist-Shannon sampling theorem, its importance and relevance. [4 marks]

b) The 556 IC chip is a voltage-controlled oscillator that provides oscillations whose frequency can be adjusted over a range controlled by a DC voltage. The operating data of a 556 IC chip is given below:

$$2\,\text{k}\Omega < R_1, R_4 < 20\,\text{k}\Omega \quad ; \quad 0.05\,V^+ \leq V_c \leq V^+ \quad ; \quad f_o \leq 1\,\text{MHz} \quad ; \quad 5\,\text{V} \leq V^+ \leq 30\,\text{V}$$

The voltage $V_c$ is the modulating input voltage, and $f_o$ is the center-operating frequency given by

$$f_o = \frac{1}{R_1 C_1}\left(\frac{V^+ - V_C}{V^+}\right)$$

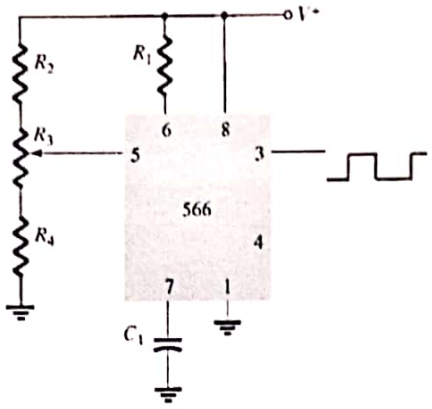


Figure 5: Phase-Locked Loop (PLL)

Given a of a 24V power supply, design a voltage-controlled oscillator (i. e. choose values for $R_1$, $R_2$, $R_3$, $R_4$, and $C_1$) that meets the following specifications. [9 marks]

- 110 $k$Hz center-operating frequency at a DC bias-point midway the allowed operating range.
- A 10:1 frequency range of operation about the 110 $k$Hz center-operating frequency.